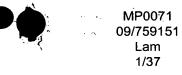
09759151.091902



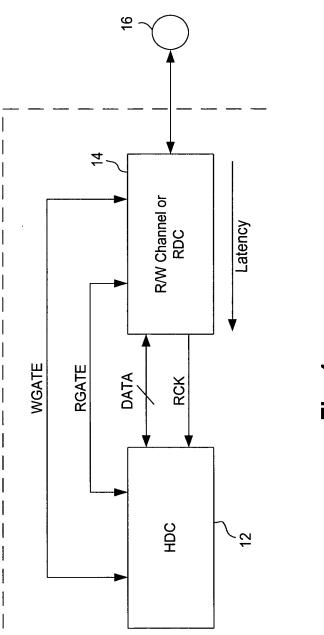


Fig. 1

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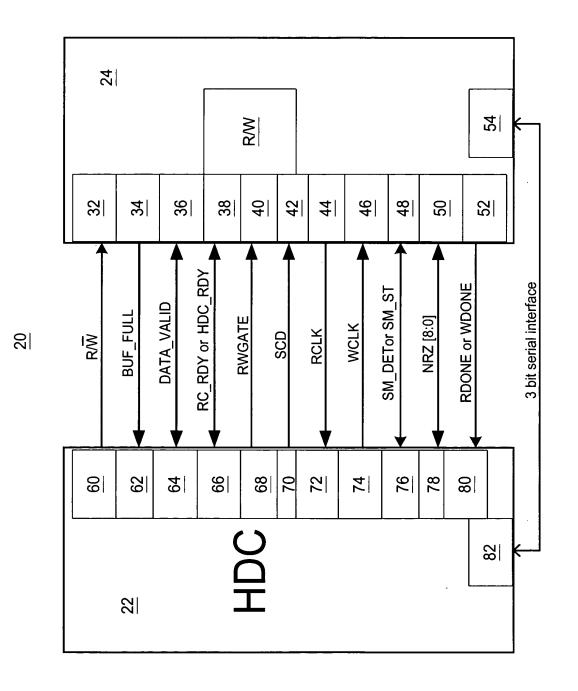


Fig. 2



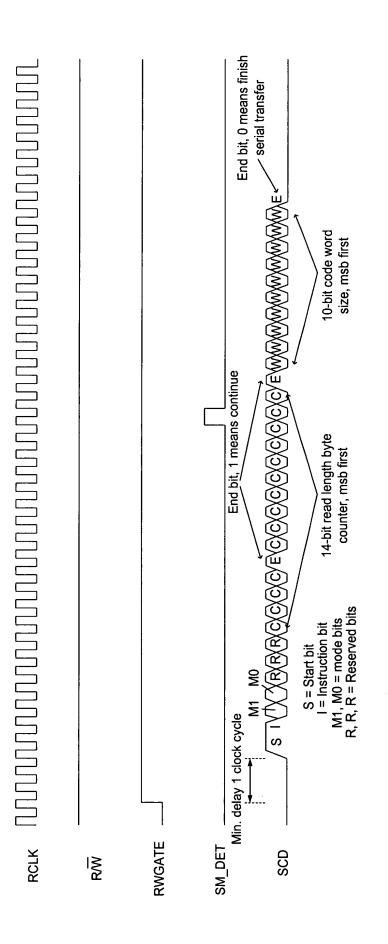


Fig. 3

Min. delay 1 clock cycle

SM_DET

RWGATE

R M

RCLK

S = Start bit I = Instruction bit M1, M0 = mode bit

SCD



MS MS

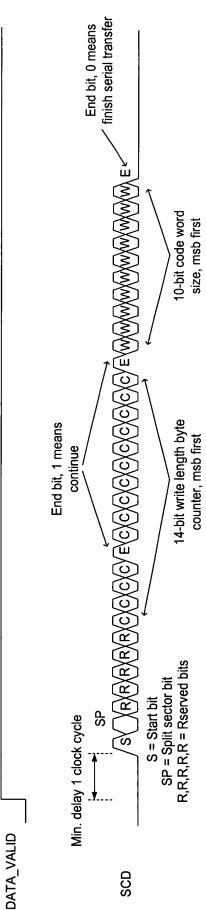
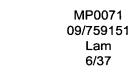


Fig. 5





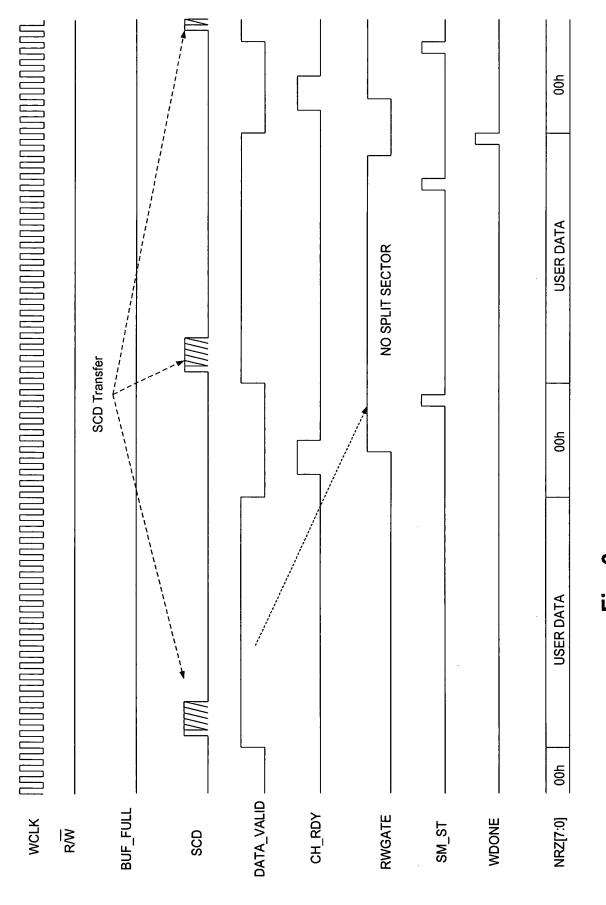


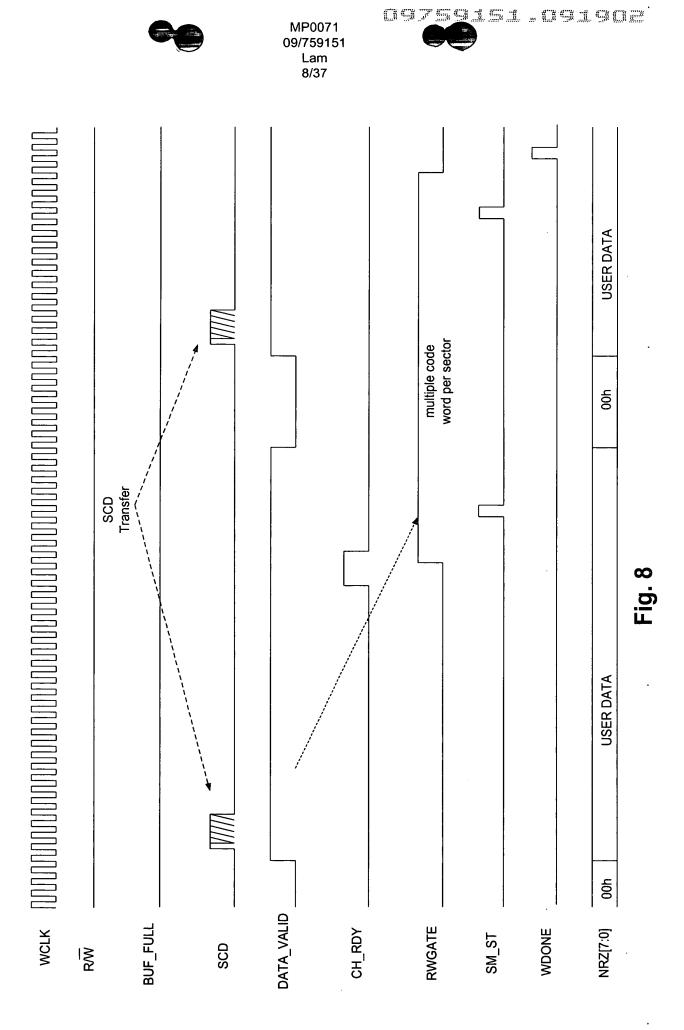
Fig. 6

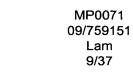


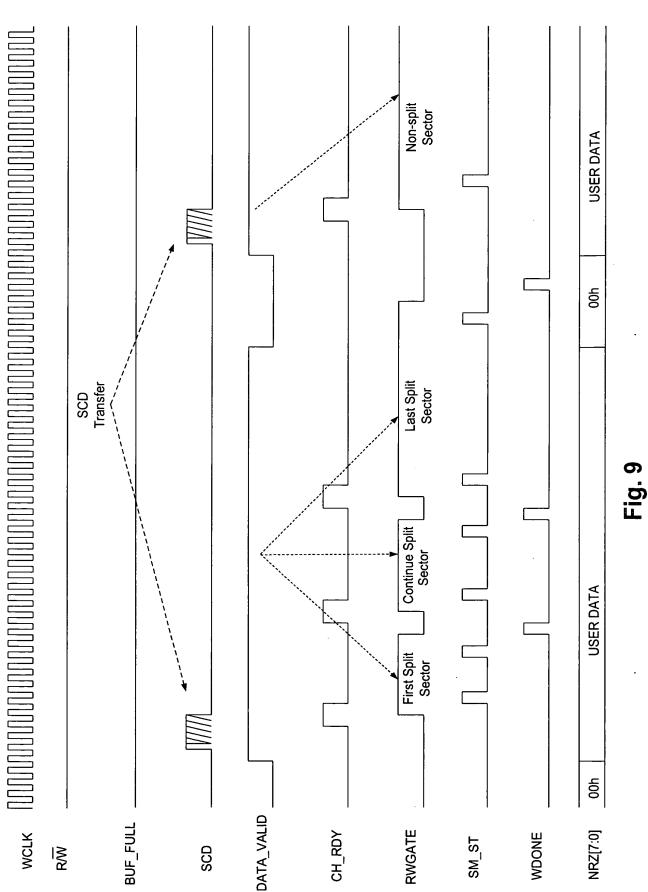
MP0071 09/759151 Lam 7/37

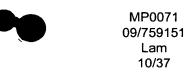
No Split Sector 9 Split Sector **USER DATA** SCD Transfer Split Sector 9 **USER DATA** 9 DATA_VALID CH_RDY BUF_FULL SM_ST **RWGATE** WDONE NRZ[7:0] SCD R Me

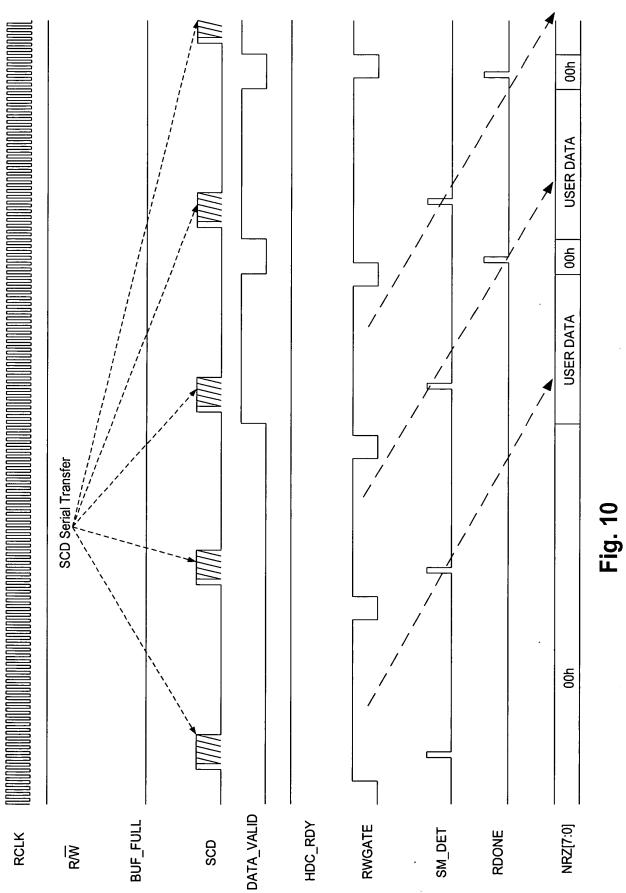
Fig. 7











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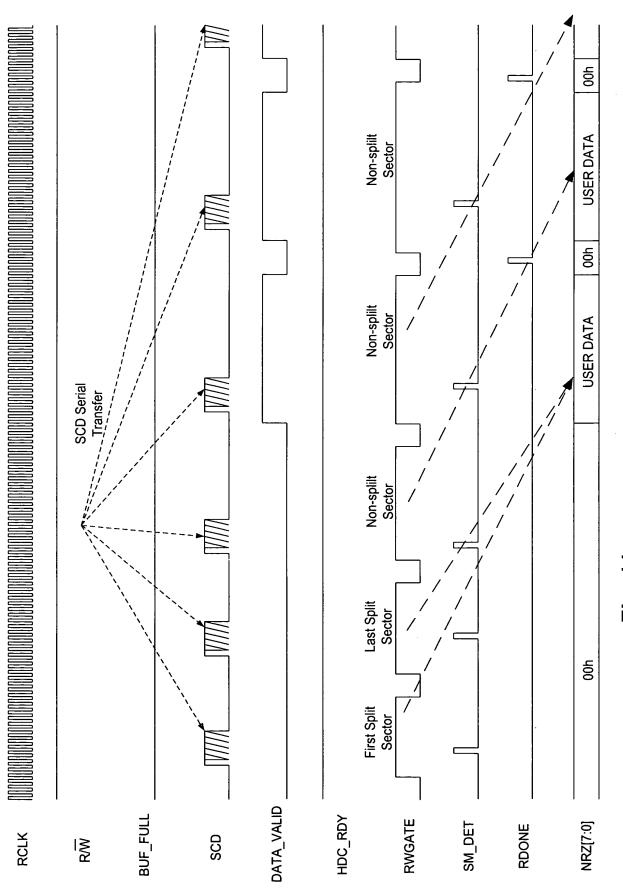
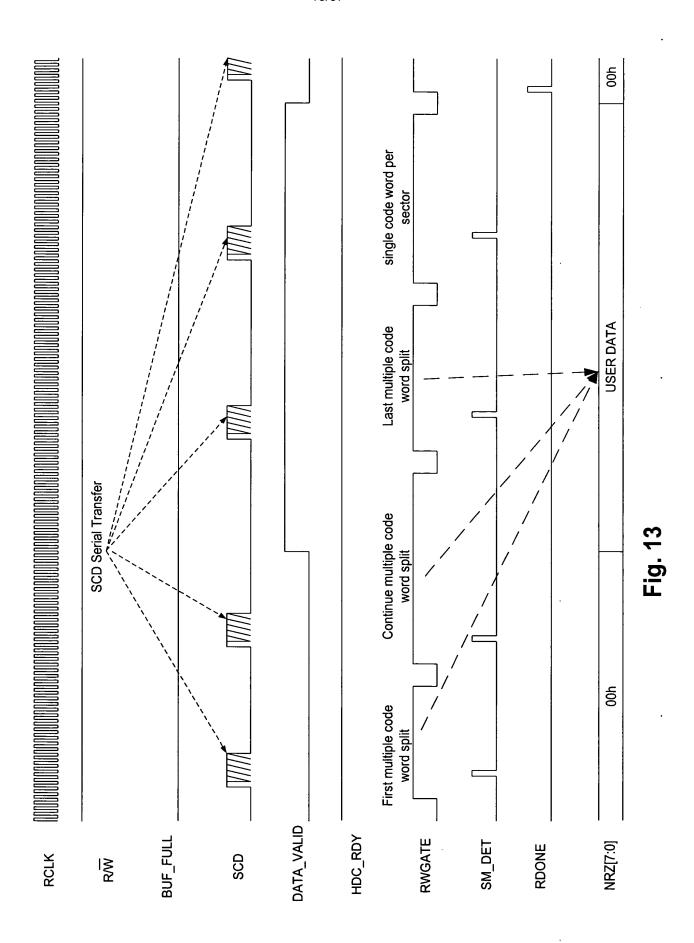


Fig. 11

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24'

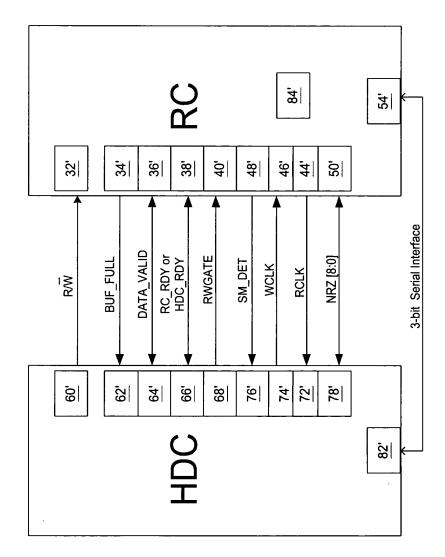
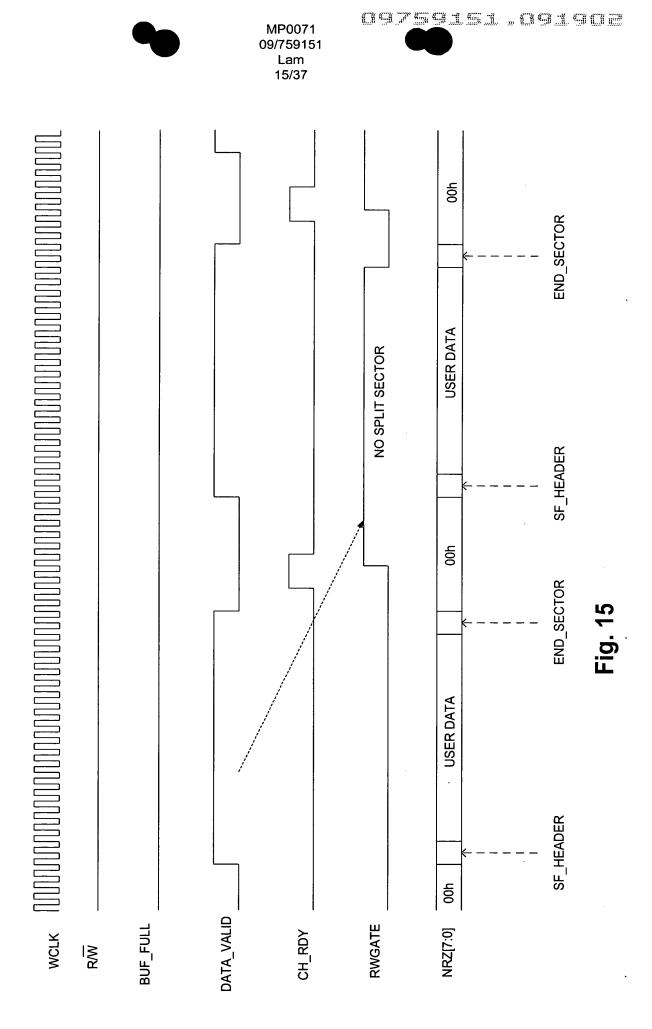
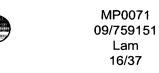


Fig. 14

20,





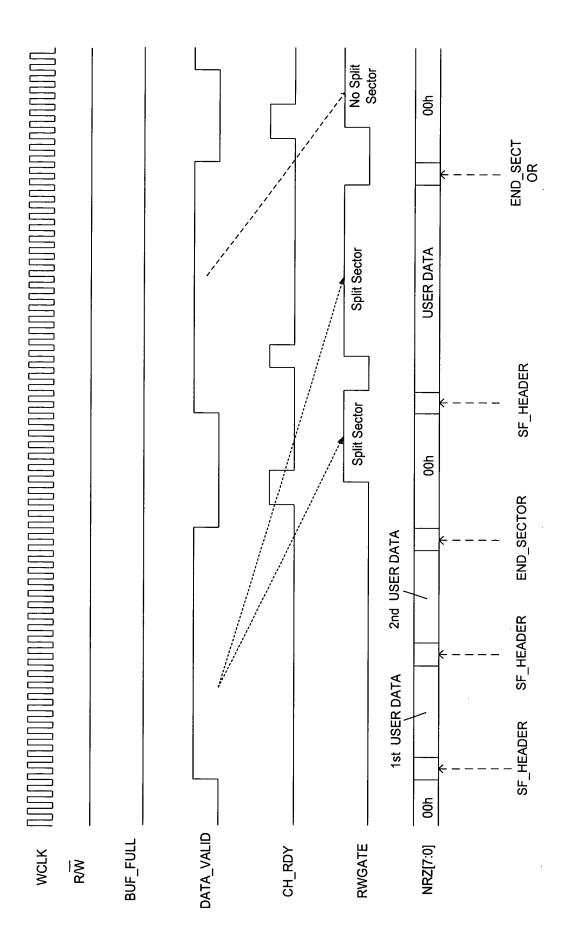


Fig. 7

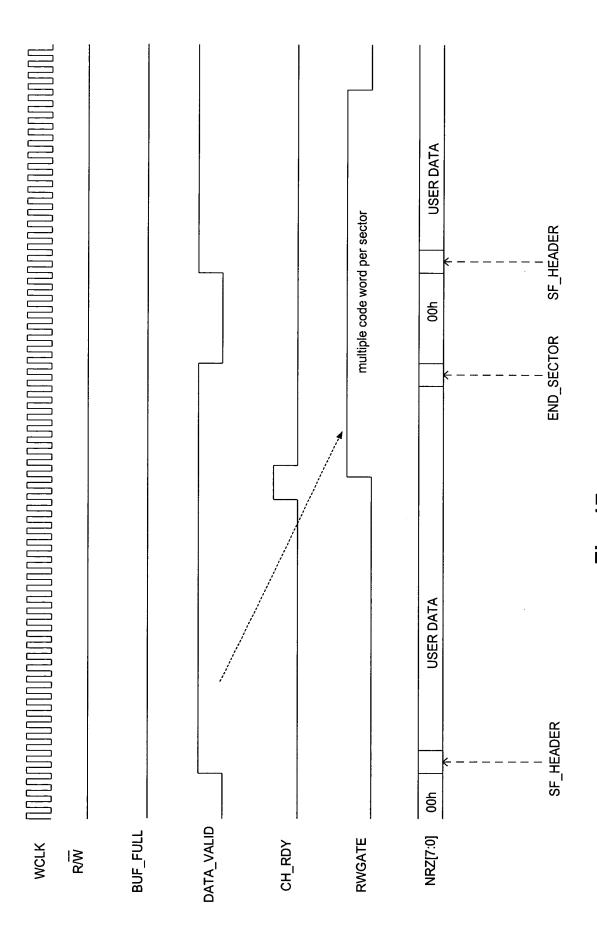
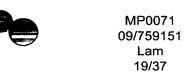


Fig. 17

Non-split Sector **USER DATA** SF_HEADER 9 END_SECTOR Last Split Sector 3'rd USER DATA SF_HEADER 2'nd USER DATA Continue Split Sector SF_HEADER 1st USER DATA First Split Sector SF_HEADER 6 DATA_VALID BUF_FULL CH_RDY **RWGATE** NRZ[7:0] R M

Fig. 18



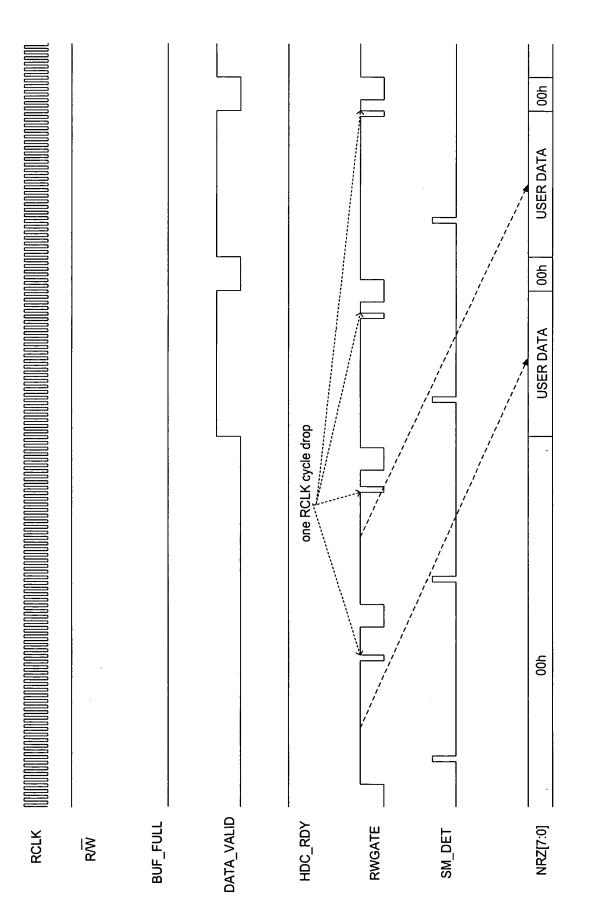


Fig. 19

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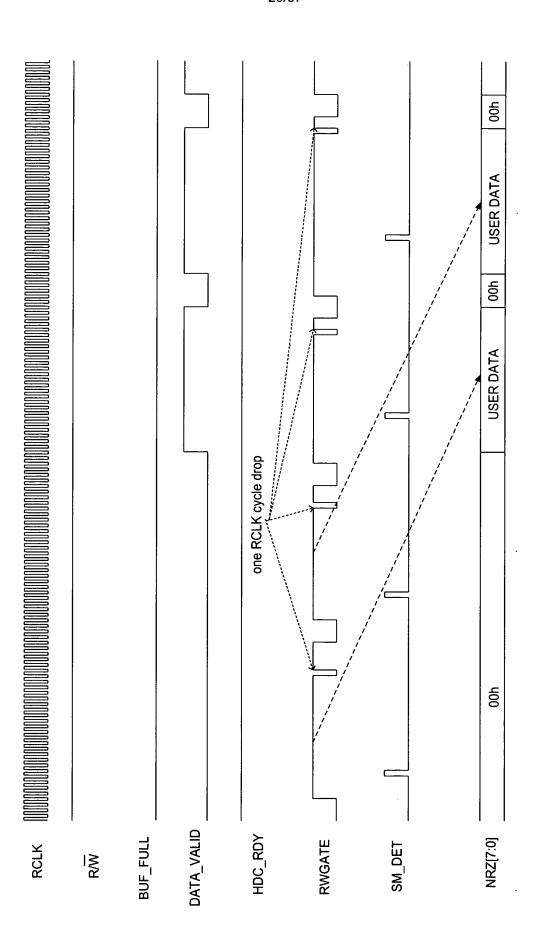
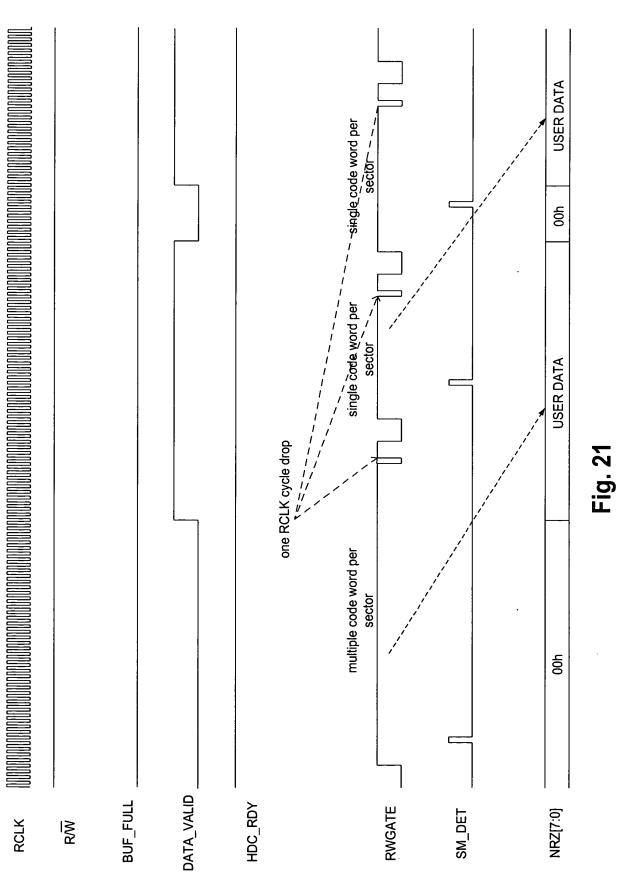


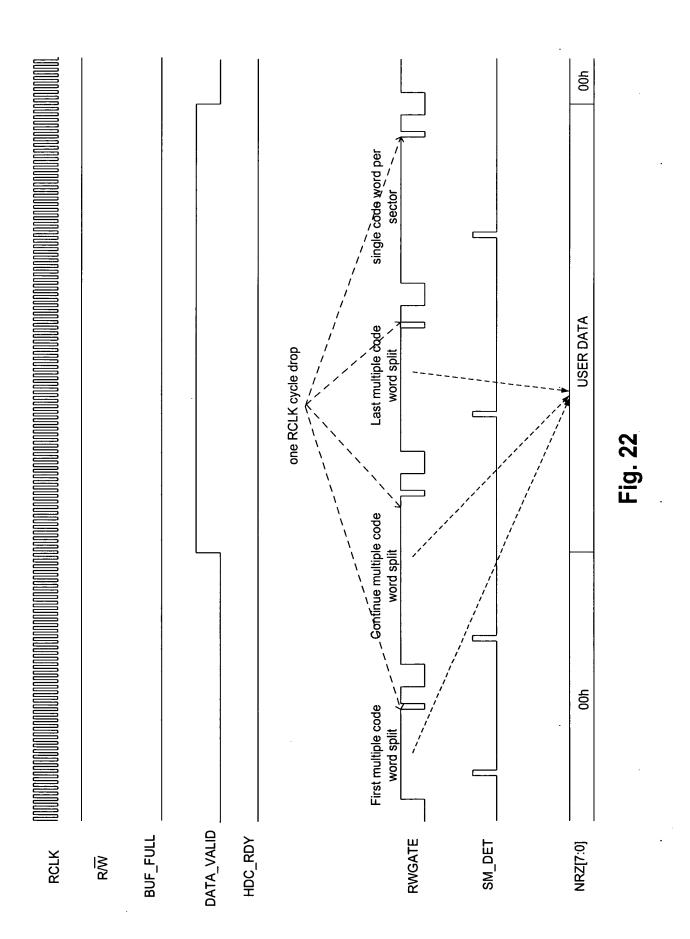
Fig. 20

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SF_HEADER User data for Multiple codewords END_SECTOR

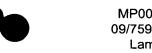
Fig. 23

SF HEADER	1st set	SF HEADER	2nd set	SF HEADER	3rd set	END SECTOR
-	user data	I	user data	I	user data	

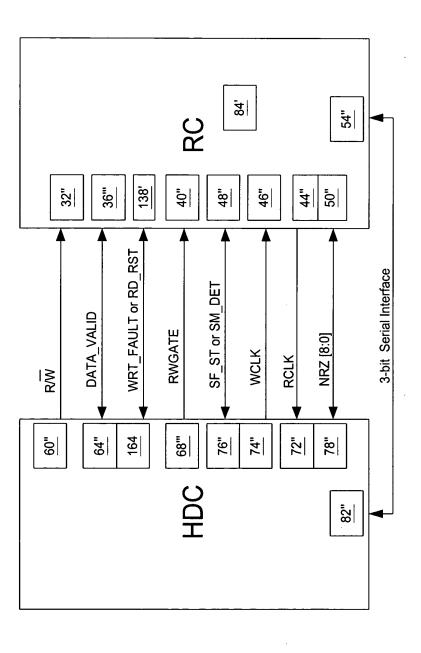
Fig. 24

Bigo Dago

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24"



20"

22"



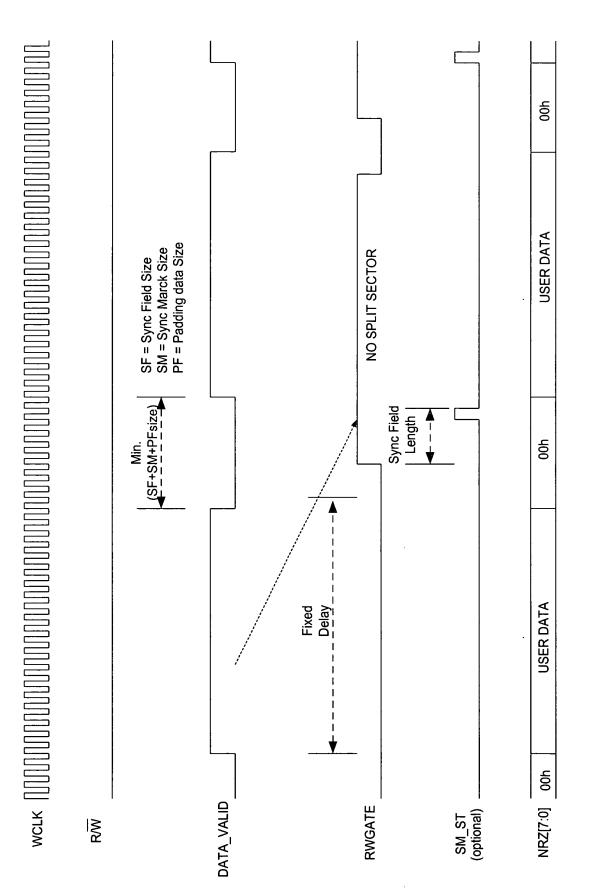


Fig. 26

Split Sector Sync Field Length min (SF+SM+PF) *2 **A** 9 2nd USER DATA **Fixed Delay** 1st USER DATA 90 H DATA_VALID SM_ST (optional) NRZ[7:0] l§ RWGATE

Fig. 27



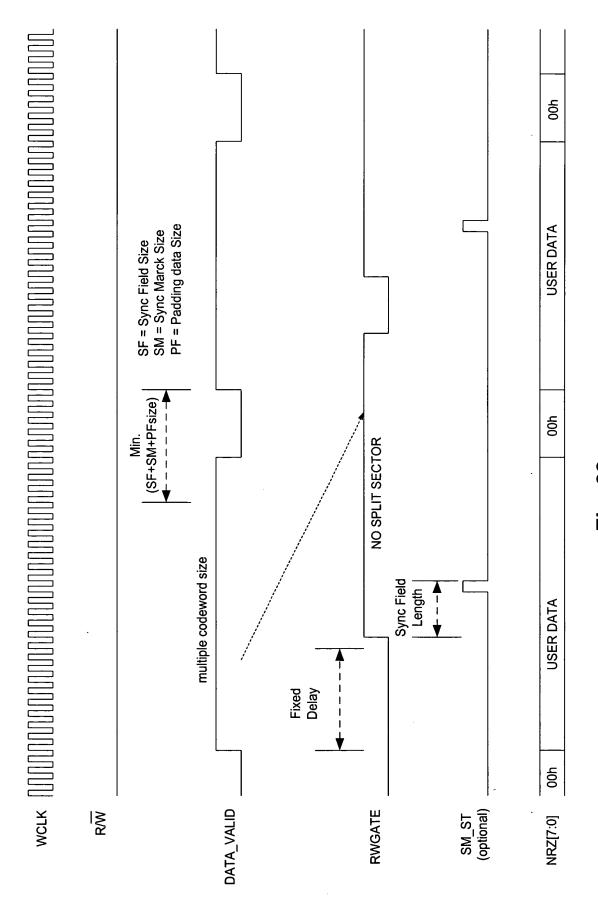


Fig. 28



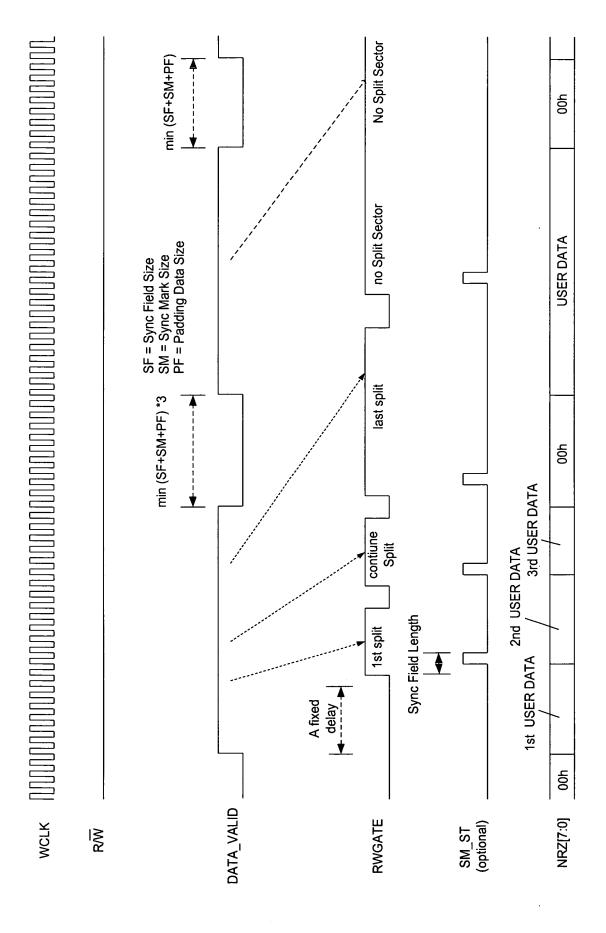


Fig. 29

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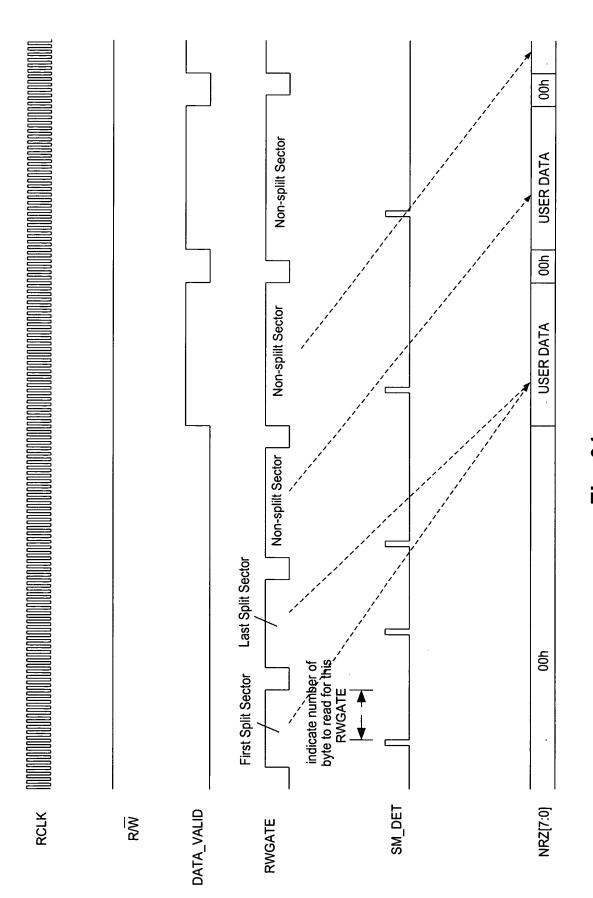
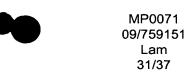


FIG. 31



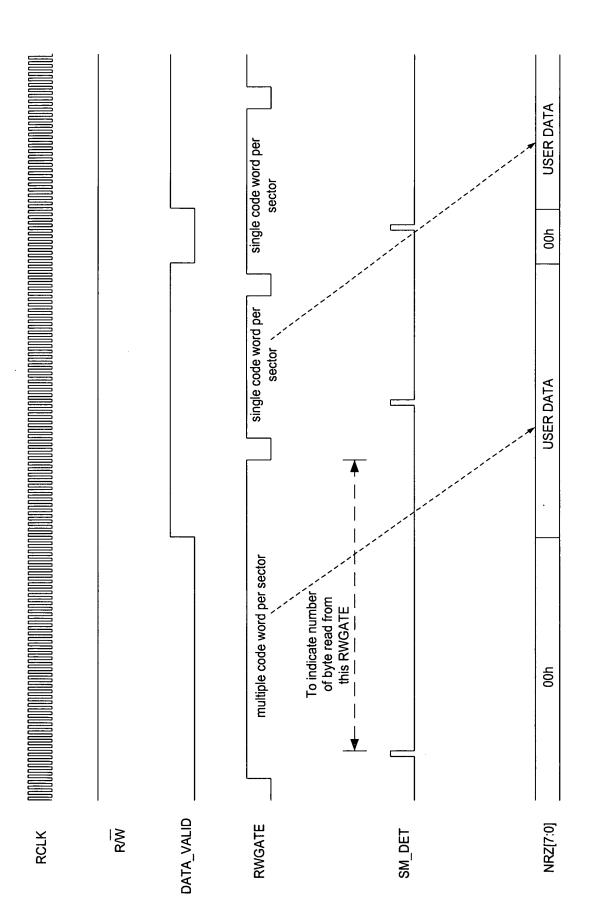


Fig. 32



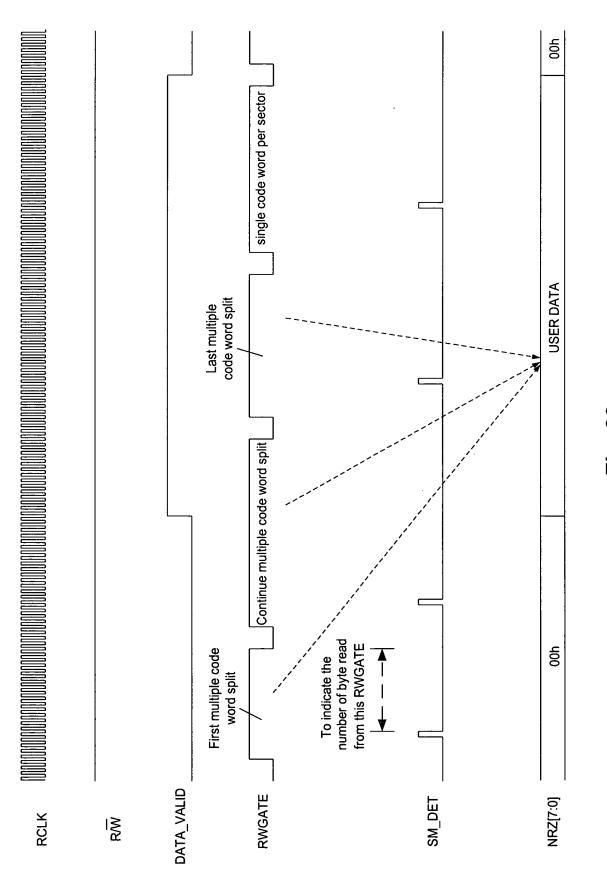
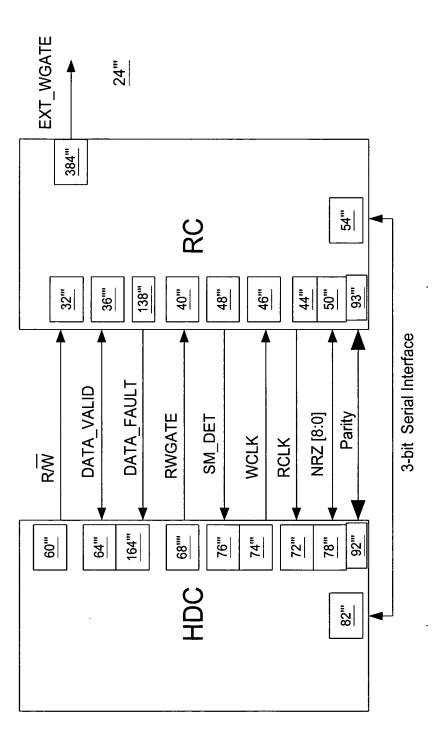


Fig. 33

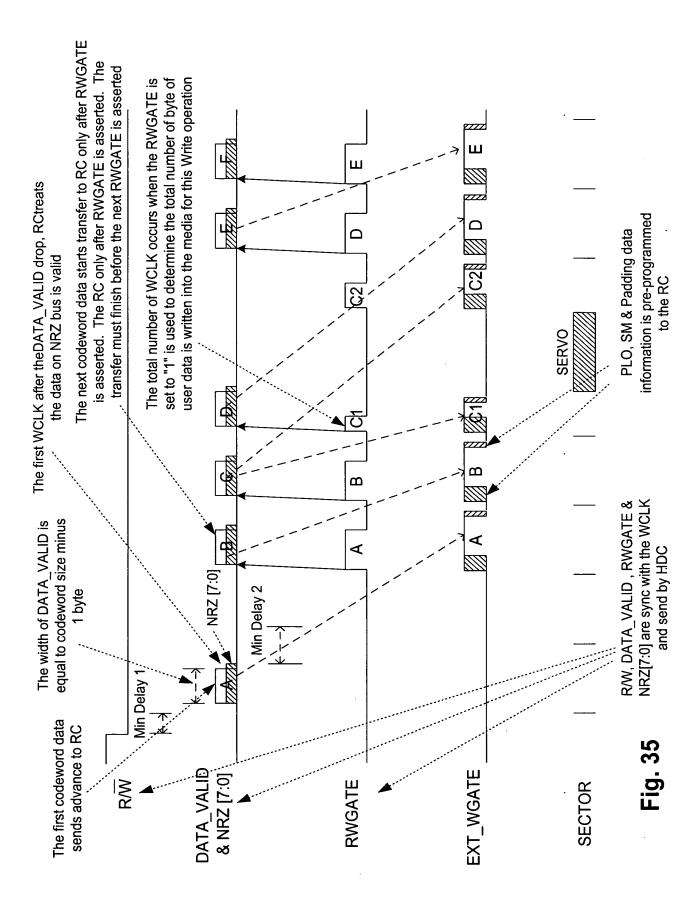




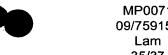
ig. 34

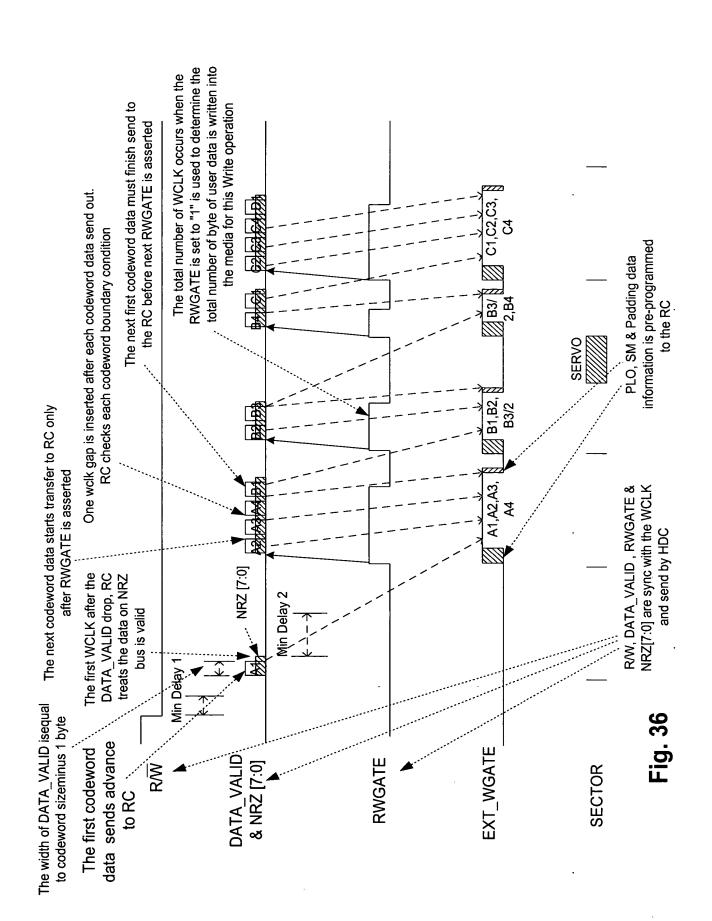
20...

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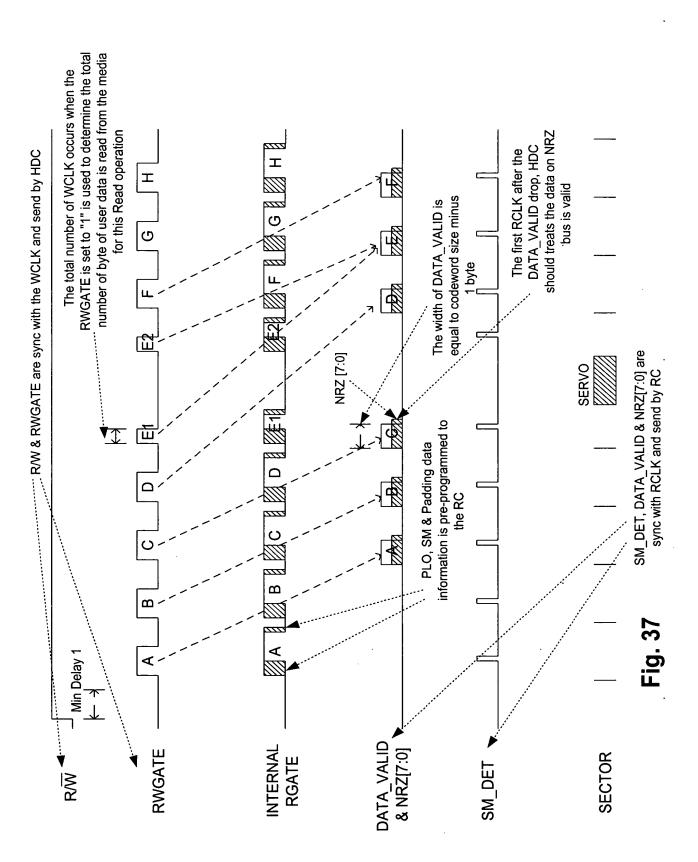
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MP0071 09/759151 Lam 36/37





MP0071 09/759151 Lam 37/37

